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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER

TRINH, MICHAEL MANH

ART UNIT

PAPER NUMBER

2822

DATE MAILED: 03/13/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Applicati n No.

09/740,174

Applicant(s)

PORTER ET AL.

Examiner

Michael M Trinh

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-- Th MAILING DATE of this communication appears on the cov r she t with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 5/22/02 & 12/19/02.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 35-38 and 42-62 is/are pending in the application.
- 4a) Of the above claim(s) 38 and 42-50 is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 35-37 and 51-62 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.
If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
* See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☒ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- 1) ☐ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 5.
- 4) ☐ Interview Summary (PTO-413) Paper No(s). _____.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____.

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DETAILED ACTION

*** This office action is in response to Applicant's amendment and election filed on May 22, 02. Claims 35-38,42-62 are currently pending.

*** Claim 62 is objected for containing typographical error. In claim 62, line 3+, "each source of the plurality of second type transistor is coupled to the drain..." should be, "each drain of the plurality of second type transistor is coupled to the drain...", and thus, "each drain of the plurality of second type transistors is coupled to the second voltage input" should be "each source of the plurality of second type transistors is coupled to the second voltage input" (Fig 4B).

Election/Restriction

1. Applicant's election filed May 22, 2002 of method claims 35-37 in Paper No. 7, with traverse, is acknowledged. The main traversal is on the ground(s) that "the only support given for this assertion is an indication of PTO classification... Species ... falling into class 438 ... subclass 238..., subclass 241... are all indented under subclass 197..." and "...Species 'b' [claim 35] is generic to [other] Species....".

This is noted and found unconvincing. First, as already reasoning and pointing out in the restriction that, for examples, Species 'b' is directed to form a "first inverter", while Species 'c' is differently directed to form "the first and second inverter"; while Species 'g' is differently directed to form "a memory cell including forming a pull up transistor and a pull down transistor", while Species 'i' is differently directed to form "a SRAM device including a plurality of row and column", etc.. Although different processing steps are not expressly mentioned in the restriction, distinct processing limitations for making these Species are apparent from the claims and can be incorporated in the restriction, but not expressly included in the restriction for the reasons of reading simplification. Applicant further traversed that the restriction is improper because some subclasses are all indented under one subclass, or having the same subclass. In response, for an application filed with a plurality of patentably distinct species of the inventions, the restriction requirement is still proper even all these species are classified in the same class and under the same subclasses. Indeed, for a same product device, there are many distinct methods classified in the same subclass for making such product device. Examining and

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searching all of these multiple distinct species of the invention in a single case would positively put a serious burden on the examiner and to the Office. The restriction is proper and required because having a plurality of distinct species, not merely because of "different classification". Different classifications are shown to further enhance the proper restriction for some species, in which the distinct inventions have acquired a separate status as shown by different classifications, in which the fields of search are not co-extensive and separate examination would be required. Applicant further remarked that claim 35 is generic to other species. In response, this is noted and found unconvincing. If claim 35 is generic claim to other species, then, for example, species claim 38 species must include all the limitations of the generic claim 35. However, as can be seen, claim 38 does not include "coupling the first contact to a first voltage input; coupling a second contact to the first source". The requirement is still deemed proper.

2. Claims 38,42-50 are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected invention, there being no allowable generic or linking claim.

Specification

3. The disclosure is objected to because of the following informalities:

** At line 25, line 27, and line 28 of page 20, the terms "32 and 34" should be --32 and 36-- since "34" is pull-down transistors.

** At line 1, page 21, the term "pull-down transistors 36,38" should be --transistors 34,38--, since the transistor "36" is pull-up transistor.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

4. Claims 57,60-62 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

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It is unclear and confusing since fabricating of a first inverter as recited in the preamble of claim 35 does not have a plurality of first type transistor in the well and a plurality of second type transistors outside the wells as in claims 57,60-62.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

- (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.
- (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
- (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

6. Claims 35-37,51-62 are rejected under 35 U.S.C. 102(b) as being anticipated by Canaris et al (5,406,513).

Canaris et al teach a method for forming a SRAM memory cell having an inverter comprising at least the steps of: providing a semiconductor of a first type conductivity; forming a well 18 of a second conductivity type in the semiconductor 10; forming a first type transistor in the well, wherein the first type transistor has a first source “S” 22, a first drain “D” and a first gate 30 “G” (Figs 3,4A,4B; col 3, line 28 through col 4; col 2, lines 18-31); forming in the well a first contact 40 in spaced relation to the first type transistor; forming a second contact 40 in the well in spaced relation to the first type transistor; coupling the first contact to first voltage input; and coupling the second contact 40 to the first source 22 to a same common potential line. Re claim 36, wherein the first left contact 40 separated from the first source 22 by a first distance defining a first parasitic resistance, and wherein the second right contact 40 separated from the first source 22 by a second distance defining a second parasitic resistance (Figs 3,4A). Re claim 37, wherein an N-well is formed in a P-type semiconductor substrate (col 3, lines 45-54; col 2, lines 34-55), and so that the first type transistor comprises a first p-type region in the well defining the first source, a second p-type region in the well defining the first drain, and a gate

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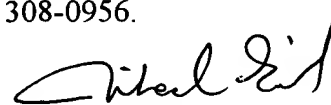
over the well. Re claims 51-52, wherein coupling the first source to the second contact comprising forming a metallization interconnect layer over the semiconductor substrate (Figs 3,4A; col 5, lines 47-58). Re claims 53,54, wherein the first source 22 is coupled to the first voltage input through a parasitic resistance $R_w, R'_w, R's, R_s$ of the well (Figs 4A-4B; col 3, line 28 through col 4), and wherein the first source is coupled to the first voltage input through the series combination of the first and second components of parasitic resistance. Re claims 55-56, wherein the distance from the first left contact 40 to the second right contact 40 is greater than distance from the first contact to the first source 22 (Figs 3,4A), and re claim 56, wherein the first type transistor is between the first and second contacts. Re claims 58-60, wherein forming a second type pull down transistor outside the well, coupling the transistor to a second voltage input, and coupling the semiconductor substrate to a third voltage input comprising a substrate tie contact 42 proximate to the second transistor (Figs 3,4A), wherein the first transistor comprises a pull up transistor, and the second transistor comprises a pull down transistor. Re claims 57,61-62, wherein a plurality of first type transistor are formed in the well (Figs 6A-6B;3,4A-4B), each transistor including a source, a drain, a gate, coupling to the second contact, wherein a plurality of second type transistors are formed outside the well, coupling to the second voltage input, wherein each of the second transistors has source, drain and gate, wherein each drain of the first type transistor coupled to each drain of the second type transistor (Figs 4A,6A-6B, and each source of the second transistors is coupled to the second voltage input (Figs 4A,6A-6B).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael M. Trinh whose telephone number is (703) 308-2554. The examiner can normally be reached on M-F from 8:30 Am to 4:30 Pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on (703) 308-4905. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7722 for regular communications and (703) 308-7724 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

Oacs



Michael Trinh
Primary Examiner